

Program 1st July

ARCHITECTURE DAY

- 08:30-09:00 **Registration & coffee**
Welcome Chris Jesshope from the University of Amsterdam
- 09:00-10:30 Industry session
Homogeneous Multiprocessing for consumer electronics
By Paul Stravers, from Philips Research Eindhoven
Optimising the power consumption of a system on chip by exploiting the trade-off between concurrency and centralized control
By Vasekin from ARM Ltd.
SVEN-Scaleable Video Engine for the DTV market
By Gerald Krottendorfer and Rumman Syed from On Demand Microelectronics Vienna
- 10.30-11:00 Discussion
- 11:00-11:30 Coffee
- 11:30-12:30 Product slot –industry
Deterministic Parallel Processing (with demo)
By Gajinder Panesar from PicoChip Designs Ltd. Bath
- 12:30-14:00 **Lunch**
- 14:00-15:30 Research session
The challenges of Massive On-chip Concurrency
By Kostas Bousias and Chris Jesshope from University of Amsterdam
A Case for Chip Multiprocessors based on the Data-Driven Multithreading Model
By Paraskevas Evripidou and Pedro Trancoso from the University of Cyprus
- 15:30-16:00 Discussion
- 16:00-16:15 **Coffee**
- 16:15-17:30 *Scalable and Partitionable Asynchronous Arbiter for Micro-threaded Chip Multiprocessors*
By N.M. Hasasneh and I.M. Bell from the University of Hull and C.R. Jesshope from the University of Amsterdam
Matrix Register File and Extended Subwords: Two Techniques for Embedded Media Processors
By Ben Juurlink of the University of Delft
Gaussian Interconnections for On-chip Networks
By Ramon Beivide from the University of Cantabria
From Maurer Computers to Micro-threads
By Jan Bergstra, Inge Bethke, and Alban Ponse from the University of Amsterdam and Kees Middelburg from....
- 17:30-18:00 Discussion
- 19:30- ?? **Workshop Dinner**

Program 2nd July

COMPILER DAY

08:30-09:00

Coffee

09:00-10:30

Industry session

Plumbing by Compilation

By Marcel Beemster from ACE Associated Compiler Experts
Amsterdam

Compiling multi-core and many-core on chips

By Jesse Fang Director Programming Research Lab Intel

*Developing System Software on many-core-on-a-chip
architectures: A case study*

By Prof. Gao from the University of Delaware

10:30-11:00

Discussion

11:00-11:30

Coffee

11:30-12.:30

Product slot – academic

A Language Design for Multi-Threaded Execution

By Clemens Greck from the University of Lubeck and Sven-
Bodo Scholz from the University of Hertfordshire

A Hybrid Execution Model for SaC

By Clemens Greck and Sven-Bodo Scholz

12:30-14:00

Lunch

14:00-15:00

Research session

*CAR-SoC-Techniques for Connective, Autonomic, Real-time
Systems on Chip*

By Sascha Uhrig and Theo Ungerer from the University of
Augsburg

*sNet: a type-directed coordination paradigm for streaming
networks*

By Shafarenko from University of Hertfordshire

*Characterization of legal transformation sequences for
modern architectures*

By Christine Eisenbeis and Nicolas Vasilache from INRIA

15:00-15:30

Discussion

15:30-15:45

Coffee

15:45-16:45

*The Challenges of Efficient Code Generation for Massively
Parallel Architectures*

By M.M. Guinness, O.Egan and B.Christianson from the
University of Hertfordshire

Enabling SMT processors for real time systems

By Peter Knijnenburg from the University of Leiden

Discussion